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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/443,883	11/18/1999	JEROME BOMBAL	VL5-062	7906

24738 7590 12/22/2004

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION  
INTELLECTUAL PROPERTY & STANDARDS  
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SAN JOSE, CA 95131

EXAMINER

THOMSON, WILLIAM D

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/443,883

Applicant(s)

BOMBAL ET AL.

Examiner

William Thomson

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date: \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. Claims 1-25 of U.S. Application 09/443,883 are pending.

#### **Claim Interpretations**

2. The broadest reasonable interpretation of the claim language has been given to the claims. It is interpreted that the claimed invention pertains to the simulation of scan path functionality.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

4. A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Barch et al. ('853).

6. Barch et al. disclose a method to test an integrated circuit design on a computer simulation loads a desired simulation test vector in parallel into a scan chain. The simulation loads the desired vector at a slight offset or upstream shift allowing several serial shifts of the loaded vector through the scan chain (32). After the serial shifts, the initial IC state is set for executing an IC function. The IC function includes applying an input on the external pins and receiving an output from the external pins, given the initial IC state loaded by the simulation. After executing the IC function, the simulation unloads the resulting IC state in parallel and compares the resulting IC state to a target vector

Barch et al. further disclose testing IC designs via computer simulation of scan path testing. The testing of an IC design on a computer simulation using parallel ATPG test patterns proceeds as follows. The simulation sets some or all of the individual states of internal elements by loading in parallel a desired initial IC state generated by the ATPG. The simulation then simulates a functional operation of the IC by providing a simulated input vector to the external pins of the IC design and receiving a simulated output vector from the external pins. In the course of simulating normal operation, the IC state changes. The simulation completes the testing by comparing the new IC state to a desired or target IC state generated by the ATPG. Since the IC design is simulated, the computer simulation has access to internal elements and can load and unload the scan chain in parallel. In particular, see figure 1 and corresponding text.

### ***Response to Arguments***

7. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

### **Conclusion**

8. **Any inquiry concerning this communication or earlier communications from the examiner should be:**

**directed to:**

William Thomson, telephone number (703) 305-0022, Monday-Thursday 0830 to 0700 ET,

**or** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

**mailed to:**

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Commissioner of Patents and Trademarks  
Washington, D.C. 20231

**or faxed to:**

(703) 308-9051 (for formal communications intended for entry)

**or** (703) 308-1396 (for informal or draft communications, please label "*PROPOSED*" or "*DRAFT*").

William Thomson

Primary Patent Examiner

December 11, 2004

*Hugh Jones*  
HUGH JONES  
PRIMARY PATENT EXAMINER  
TECHNOLOGY CENTER 400  
*Sor William Thomson*